Filing Date: August 30, 2001

Title: HIGHLY RELIABLE AMORPHOUS HIGH-K GATE OXIDE ZrO2

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REMARKS

This responds to the Office Action dated on November 27, 2006.

Claims 1, 9, 14, 22, 30, 51 and 55 are amended, claims 5, 13, 18, 26 and 34 are canceled, and no claims are added; as a result, claims 1, 2, 6-10, 14-15, 19-23, 27-31, 35-37, 51, 52, 54-56, and 62 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 2, 5-7, 14, 15, 18-20, 51, 52, 55, 56 and 62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808) and Yano et al. (U.S. Patent No. 5,810,923). Applicant respectfully traverses this rejection.

The cited references have all been previously discussed. Ma discloses a metal oxide gate dielectric formed of Zr or Hf alloyed with approximately 25% of a trivalent metal such as aluminum or lanthanum, formed by sputtering in an oxygen ambient. Ma suggests an interface barrier 62 of 2-5 Å of silicon nitride or silicon oxynitride (col. 2, line 17 and col. 6, line 9 and figures 12 and 13). Park is used to show that sputtering and evaporation are art recognized equivalents. Yano is used to show that the deposition temperature range, the use of atomic oxygen, and that smooth metal oxide surfaces are known.

The Examiner concedes on page 12 of the outstanding Office Action that there is a difference between sputtering and evaporation, at least in surface roughness. Applicant respectfully submits that the Examiner is incorrect in asserting that there could be motivation in combining a reference such as Ma that does not suggest either electron beam evaporation or that there is a surface damage and roughness problem with sputtering, with a reference such as Park which also suggests that sputtering and evaporation are equivalent and has no suggestion of surface damage and roughness problems. Applicant wonders what portion of the cited references would provide the suggestion to arrive at the present method? The present specification at page 6, line 18, and page 7, line 20, contrasts the use of a thermal evaporation technique for smooth surfaces and minimal unwanted silicides and oxides, as found in the cited Ma reference, to improve the surface smoothness (col. 6, lines 9-11).

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The Examiner concedes on page 13 of the outstanding Office Action that Ma does teach metal oxides with 25% trivalent metals such as aluminum, but argues that the use of a single metal is known. Applicant respectfully submits that none of the references provide any possible suggestion of a benefit to using a pure single metal for forming a smooth thin layer for oxidation into a smooth thin dielectric layer, as found in the present claimed method. Applicant submits that no ordinary skilled worker would be motivated to use extremely pure metal layers when reviewing references suggesting up to 25% mixed metals, or not suggesting pure metals. One of ordinary skill in the art would not understand Ma to be teaching a pure metal, since Ma teaches the use of a trivalent metal alloy, which can not suggest the use of very pure materials. Applicant submits that a suggestion of not intentionally adding a trivalent material does not suggest the use of highly purified metals, and requests the Examiner to specifically point out where such an objective suggestion might exist, as required under 35 USC § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988).

On page 13 of the outstanding Office Action the Examiner argues that Ma does not teach that the insulator layer includes an interface barrier 62 of silicon nitride or silicon oxy-nitride, and that the barrier is optional. Applicant submits that the barrier layer 62 is shown in every figure showing the gate dielectric and even has a specified thickness 64, and is stated to provide at least the benefit of improving "electron mobility of the MOSFET" (see col. 2, line 13; col. 6, line 10). Applicant submits that one of ordinary skill would not be motivated to change the teaching of Ma to obtain the present claimed arrangement of direct contact of the metal with the body region (see page 7, line 26).

Specifically, Applicant respectfully submits that the suggested combination of Ma with Park and Yano fails to describe or suggest at least the claimed feature of a "...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting a single crystal semiconductor portion of the body region using electron beam evaporation at a temperature between 150 to 200 °C...", as recited in independent claim 1, as amended herein. The cited references do not suggest pure metal, evaporation in preference to sputtering, or directly contacting the semiconductor body region. Independent claims 9, 14, 22,

30, 51, 55 and 62 are held to be patentable over the suggested combination of references for similar reasons.

The dependent claims are held to be in patentable condition at least as depending from base claims shown above to be patentable over the suggested combination of references. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 8-10, 13, 21 and 54 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589), Park (U.S. Patent No. 5,795,808) and Yano et al. (U.S. Patent No. 5,810,923) as applied to claims 1, 2, 5, 6, 14, 15, 18-20, 51, 52, 55, 56 and 62 above, and further in view of Moise et al. (U.S. Patent No. 6,211,035). Applicant respectfully traverses this rejection.

The features of Ma, Park and Yano are discussed above. Moise is used to show that oxidizing in an inert ambient is known.

Applicant submits that the addition of the features of the Moise reference does not cure the above-noted deficiencies in the combination of Ma, Park and Yano with regard to independent claims 1, 14 and 51, from which the claims in question depend. The combination does not suggest direct metal contact to the body region, use of pure metal, or the substantial amorphousness of the deposited metal, none of which features is addressed in Moise.

Applicant respectfully submits that the suggested combination of references fails to describe or suggest at least the claimed feature of a "...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting a single crystal semiconductor portion of the body region using electron beam evaporation at a temperature between 150 to 200 °C...", as recited in independent claim 1, as amended herein.

The other independent claims are held to be patentable for similar reasons. The dependent claims are held to be in patentable condition at least as depending from base claims shown above to be patentable over the suggested combination of references. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 22, 23, 25-28, 30, 31 and 33-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No.

5,795,808), Yano et al. (U.S. Patent No. 5,810,923) and Maiti et al. (U.S. Patent No. 6,020,024), furthermore in view of the admitted prior art (pages 1-4). Applicant respectfully traverses this rejection.

The references of Ma, Park and Yano have features discussed Above. Maiti is used to show that transistors having high dielectric constant metal oxide gates are known.

Applicant submits that the addition of Maiti does nothing to cure the failures of the other references to describe or suggest at least the features of "...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting the body region using electron beam evaporation at a temperature between 150 to 200 °C, the metal being chosen from the group IVB elements of the periodic table...", as recited in claim 22, as amended herein. The cited references fail to suggest methods to keep the surface clean and smooth, and a gate dielectric formed directly on the transistor body region. The same reasoning applies to the other independent claims.

The dependent claims are held to be in patentable condition at least as depending from base claims shown above to be patentable over the suggested combination of references. Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Claims 29 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,207,589) in view of Park (U.S. Patent No. 5,795,808), Yano et al. (U.S. Patent No. 5,810,923) and Maiti et al. (U.S. Patent No. 6,020,024) as applied to claims 22, 23, 25-28, 30, 31 and 33-36 above, and further in view of Moise et al. (U.S. Patent No. 6,211,035). Applicant respectfully traverses this rejection.

The cited references have been discussed above with reference to the prior rejections. Applicant respectfully submits that the combination of references, whether taken alone or in any combination, fails to describe or suggest at least the features of "...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting the body region using electron beam evaporation at a temperature between 150 to 200 °C, the metal being chosen from the group IVB elements of the periodic table...", as recited in claim 22, as amended herein, from which claim 29 depends.

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Applicant respectfully submits that the combination of references, whether taken alone or in any combination, fails to describe or suggest at least the features of "...evaporation depositing a substantially amorphous and 0.99999 pure single element metal layer directly contacting the semiconductor body region using electron beam evaporation at a temperature between 150 to 200 °C, the metal being chosen from the group IVB elements of the periodic table..." as recited in claim 30, as amended herein, from which claim 37 depends. The suggested combination of cited references fail to suggest pure metal directly in contact with the body region. Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Information Disclosure Statement

Applicants submitted an Information Disclosure Statement and 1449 Forms on August 17, 2006. The Examiner did not initial the non-published applications listed in the "Other Documents - Non-Patent Literature Documents" section. Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Notification of this change to this effect was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004 and October 19, 2004. Thus, Applicant has not included copies of any US Patents or US Patent Applications identifiable by serial number that may be cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

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CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at David Suhl at (508) 865-8211, or the undersigned attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

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Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 22 day of February 2007.

Name

Signature